What is claimed is:

1. An integrated circuit chip comprising embedded digital processor and an on-chip emulation device coupled to said digital signal processor, said emulation device being operable to control said digital processor and to collect information about the operation of said digital processor, the on-chip emulation device having a communication port for off-chip communication, the chip further comprising an on-chip interface having a first port connected to said communication port of said on-chip emulation device and a second port for connection to a non-proprietary bus wherein said interface is operable to convert between a format suitable for said on-chip emulation device and a format suitable for said non-proprietary bus.

2. The integrated circuit chip of claim 1 having plural embedded digital processors, each having a respective associated on-chip emulation device and a respective said on-chip interface, said integrated circuit chip further including said non-proprietary bus, and a bus connection port connected on said chip via said non-proprietary bus to the second port of each said interface.

3. The integrated circuit chip of claim 1 wherein said non-proprietary bus is a universal serial bus.

4. The integrated circuit chip of claim 3 wherein said bus connection port is a universal serial bus hub.

5. The integrated circuit chip of claim 1 wherein said non-proprietary bus is a bus complying with IEEE standard 1394.

6. The integrated circuit chip of claim 1 wherein the or each digital processor further comprises JTAG circuitry connected to said bus.

7. The integrated circuit chip of claim 6 wherein said JTAG circuitry has a further off-chip connection.

8. A method of communicating between a remote device and a digital processor, said digital processor being on an integrated circuit chip, said chip having on-chip emulation circuitry for monitoring and controlling the digital processor in response to signals from a said remote device, said chip further comprising interface circuitry disposed between a port of said on-chip emulation circuitry and a communication port for said signals, wherein said port is adapted to receive a non-proprietary bus and wherein said non-proprietary bus is adapted to convey signals having a predetermined protocol, the method comprising:

connecting said non-proprietary bus to said port and to a said remote device;

receiving said signals from said remote device over said non-proprietary bus in said non-proprietary protocol at said communication port and transferring said signals to said interface circuitry on-chip;

in said interface circuitry, converting said signals into a form suitable for said on-chip emulation circuitry, and transferring said converted signals to said on-chip emulation circuitry whereby said on-chip emulation circuitry responds to said converted signals to monitor and control said digital processor.

9. A method of debugging a digital processor using a host computer, said digital processor being on an integrated circuit chip, said chip having on-chip emulation circuitry for monitoring and controlling the digital processor in response to signals from said host computer, said chip further comprising interface circuitry disposed between a port of said on-chip emulation circuitry and a communication port for said signals, wherein said port is adapted to receive a non-proprietary bus and wherein said non-proprietary bus is adapted to convey signals having a predetermined protocol, the method comprising:

connecting said non-proprietary bus to said port and to a said host computer;

generating said signals in said host computer;

receiving said signals from said host computer over said non-proprietary bus in said non-proprietary protocol at said communication port and transferring said signals to said interface circuitry on-chip;

in said interface circuitry, converting said signals into a form suitable for said on-chip emulation circuitry, and transferring said converted signals to said on-chip emulation circuitry whereby said on-chip emulation circuitry responds to said converted signals to monitor and control said digital processor.

10. The method of claim 8 wherein said chip further comprises peripheral circuitry, and said on-chip emulation circuitry is linked to said peripheral circuitry for control and monitoring thereof.

11. The method of claim 8 wherein said non-proprietary bus is a universal serial bus and said predetermined protocol is a universal serial bus protocol.

12. The method of claim 11 wherein said integrated circuit chip further comprises JTAG circuitry connected to said interface circuitry, the method further comprising supplying test signals over said universal serial bus to said interface circuitry;
in said interface circuitry converting said test signals into JTAG protocol form; and

supplying said JTAG protocol signals to said JTAG circuitry whereby said JTAG circuitry implements boundary test functions of said chip.

13. The method of claim 12 further comprising causing said on-chip emulation circuitry to determine data illustrative of the behaviour of said chip said signals comprise interrogating signals for said on-chip emulation circuitry, whereby said on-chip emulation circuitry derives information from said data to said interface;

in said interface, converting said information into universal serial bus protocol; and transmitting said information in universal serial bus protocol over said universal serial bus to said host.

14. The method of claim 8 wherein said signals comprise program information for said EEPROM on said chip, and said on-chip emulation circuitry causes said EEPROM to become programmed in accordance with said program information

15. The method of claim 8 wherein said signals comprise program information for production programming of memory of said chip, and said on-chip emulation circuitry causes said memory to become programmed in accordance with said program information.